REMARKS

This paper is responsive to the Final Office Action dated May 19, 2004. Claims 3 - 5 are pending in this application and have been rejected. Applicant respectfully traverses the final rejection and respectfully requests reexamination.

Although this rejection is final, this is Applicant's first opportunity to discuss the rejection and the newly cited Dischert '931 reference.

Dischert '931

Dischert teaches a television display with a simple double horizontal line of video information. In Dischert each line is individually stored into a memory. The memory is then read two or more times and each line as read is displayed on a television screen, the same number of times. As explained, this is a doubling, tripling or even greater number of line repetitions. The Examiner in the outstanding Office Action at page 4, beginning at line 3 in the discussion of Dischert recognizes that Dischert teaches only storage of individual or single lines of video. The Examiner correctly recognizes that Dischert does not include a memory for an entire field, or a frame memory from which the plurality of lines are read from. In Dischert there is a delay

line (252) which becomes filled with a current line of information while delay line (254) is being read and read out (see column 3, lines 35 - 37). The timing in the memories (delay lines) is provided by switching back and forth so that one delay is loaded while the other is read out. As explained in column 3, lines 35 - 60, it is the alternate loading and reading out of delay lines (252) and (254) on a line by line basis which is disclosed.

Kawai '490

Kawai '490 shows an interlaced scan signal applied to terminal (16) shown in Figure 3 of a scanning line circuit (15). There are two FIFO field memories (17) and (18) which store interlaced scan field information. A progressive signal is generated at switch (19). Figure 4(a) shows the input interlaced scan signal at switch (16). Figure 4(b) shows the progressive output scan at switch (19). The clock rate for the progressive scan signal at switch (19) is identical to the clock rate of the input of the memories (17) and (18). Stated another way, the read out speed and read speed in memories (17) and (18) are identical. Applicant's claim 3 on the other hand, states that in reading the field signal and the field memory there is a double speed of the write speed of the signal. This is clearly not the case as shown in Figure 3 and Figures 4(a) and 4(b). The progressive signal output from switch (19) is then applied to the circuit shown in Figure 2. Circuit (15) is shown in Figure 3 discussed above. In

Figure 2, there are time compressing circuits (30) and (32). These time compressing circuits each receive progressive signal data and, as explained in the specification at column 9, beginning at line 22 and continuing through column 10, line 11, the time compressing circuits (30) and (32) in the progressive scanning system video signal provide the signal as displayed in Figure 4(c). In operation, delaying circuits (31) in combination with the timed compressing circuits (30) and (32) provides for alternately outputting the outputs of the time compressing circuits (30) and (32) in a field period of a progressive scan. As shown in Figure 4(c), this results in a progressive scanning signal where the frame rate is 60 Hz (1/60 of a second) as opposed to a case where the frame rate is only 1/30th of a second as shown in Figure 4(b). As the Examiner has recognized and was explained in the previous Office Action, '490 simply does not create the progressive scanning shown in Figure 4(c) by the claimed frame memory for storing a frame signal and reading twice the same horizontal line data of a field signal in the memory at double speed.

Applicant's Claim 1

Applicant's claim 1 is distinguishable over the combination of references in that Applicant's claim 1 recites a combination of components which must be considered as a whole wherein the combination calls for a field memory for storing a field signal for interlaced scanning. This field memory is read at double

speed of its write signal. Still further, as stated in claim 1, there is a temporary writing of this double speed signal in a frame memory. This frame memory is shown in Applicant's drawings as memory M_3. Next, claim 1 calls for controlling of the frame signal and the frame memory such that horizontal line data of the frame signal can be read twice at the double speed of a write speed of the frame signal. There is nothing like this found in or suggested by the combination of references.

As pointed out above, Dischert has only line memory, which is used for generating a plurality of lines of scan. Dischert does not include frame memory or field memory. Next, Kawai '490 does not suggest or teach the timing of the read and write control circuits found in the last paragraph of Applicant's claim 1. Namely, the reading of the field memory at double speed, the temporary writing of the signal in a frame memory, and reading of horizontal line data of the frame signal at a double speed of the write speed of the frame memory M_3.

Claim 4

Claim 4 differs from claim 1 in the recitation of the reading of the field signal in the field memory. Here it is stated that the data is read at n ($n > 3$) times as fast as the write signal. There is nothing in any of the references which would suggest this fast readout of the entire field memory to achieve the multiple lines. As pointed out above, Dischert does not have a field or a

frame memory which is read out. (Dischert has only a line memory.) On the other hand, the frame memory in Kawai is read out at exactly the same speed as it is written in. Therefore, the references when considered together do not suggest claim 4.

Claim 5

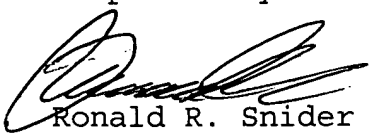
Claim 5 is similar to claim 3, except that claim 5 states that the readout speed is (n > 3) times the horizontal line data and that the frame signal can be read n times a speed n times as fast as its write signal. This phrasing of the claim is similar to claim 3, except that claim 3 recites doubling of the write speed in both memories.

Summary

Applicant has provided a progressive resolution conversion circuit which uses a field memory, a frame memory and multiple speed read and write signals which generate high density data in the vertical direction. This is a progressive resolution conversion circuit which is not suggested by or rendered obvious by the combination of references. The references taken singly do not include all of the elements of the claims as pointed out above, and still further, the references even when taken in combination do not suggest the elements of the claims, particularly the read and write speeds (or timing) in the memories.

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance, and early action in accordance thereof is requested. In the event there is any reason why the application cannot be allowed in this current condition, it is respectfully requested that the Examiner contact the undersigned at the number listed below to resolve any problems by Interview or Examiner's Amendment.

Respectfully submitted,



Ronald R. Snider
Reg. No. 24,962

Date: July 2, 2004

Snider & Associates
Ronald R. Snider
P.O. Box 27613
Washington, D.C. 20038-7613
(202) 347-2600

RRS/bam